Notice of Allowability	Application No.	Applicant(s)	
	10/668,370	ISODONO ET AL.	
	Examiner	Art Unit	
	David Ton	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/24/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Ton

DAVID TON
PRIMARY EXAMINER

Examiner Amendment

1. An Examiner's Amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 C.F.R. 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the Issue Fee.

2. Delete the ABSTRACT (which is over 150 words) and substitute therefor the new attached ABSTRACT.

3. Claims 1-12 are allowed.

4. The following is an Examiner's Statement of Reasons for Allowance:

a). The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination a logic circuit test apparatus for testing a logic circuit comprising: a common test signal generating circuit which groups the input terminals of the logic circuit on the basis of logic states of original test signals to be applied to the respective input terminals of the logic circuit and outputs common test signals from common test signal output terminals thereof smaller in number than the input terminals of the logic circuit and an input connection switching circuit which switches connections of the common test signal output terminals of the common test signal generating circuit with the input terminals of the logic circuit so as to convert the

common test signals into the original test signals and apply the original test signals to the input terminals of the logic circuit as set forth in independent claims 1 and 2.

b). The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination a logic circuit test apparatus for testing a logic circuit comprising: a common expected signal generating circuit which groups the output terminals of the logic circuit on the basis of logic states of expected signals to be outputted from the respective output terminals of the logic circuit in association with the original test signals and outputs common expected signals from expected signal output terminals thereof smaller in number than the output terminals of the logic circuit and an output connection switching circuit which switches connections of the output terminals of the logic circuit with output signal measurement terminals provided in a one-to-one correspondence with the expected signal output terminals of the common expected signal generating circuit so as to compare the output signals outputted from the respective output terminals of the logic circuit with the common expected signals as set forth in independent claim 5.

c). The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination a logic circuit test method for testing a logic circuit comprising the steps of: grouping the input terminals of the logic circuit on the basis of logic states of original test signals to be applied to the respective input terminals of the logic circuit, further grouping the grouped input terminals on the basis of logic states of the original test signals in the next cycle period, and sequentially repeating the grouping of the input terminals until the number of input terminal groups

exceeds the number of common test signal output terminals of a common test signal generating circuit smaller than the number of the input terminals of the logic circuit so as to output common test signals from the common test signal output terminals of the common test signal generating circuit and when the number of the groups exceeds the number of the common test signal output terminals of the common test signal generating circuit, generating the common test signals for corresponding respective input terminal groups provided immediately before the last grouping to the common test signal output terminals of the common test signal generating circuit as set forth in independent claims 8 and 12.

d). The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination a logic circuit test method for testing a logic circuit comprising the steps of grouping the output terminals of the logic circuit on the basis of logic states of expected signals to be outputted from the respective output terminals of the logic circuit in association with the original test signals, further grouping the grouped output terminals on the basis of logic states of the expected signals in the next cycle period, and sequentially repeating the grouping of the output terminals until the number of output terminal groups exceeds the number of expected signal output terminals of a common expected signal generating circuit smaller than the number of the output terminals of the logic circuit so as to output common expected signals from the expected signal output terminals of the common expected signal generating circuit and when the number of the groups exceeds the number of the expected signal output terminals of the common expected signal generating circuit, generating the common

expected signals for corresponding respective output terminal groups provided immediately before the last grouping to the expected signal output terminals of the common expected signal generating circuit as set forth in independent claim 10.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

6. The prior art of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached on Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton whose telephone number is (571) 272-3828. The examiner can normally be reached on M-Th from 5:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Ton
Primary Examiner
Art Unit 2138

ABSTRACT OF THE DISCLOSURE

A logic circuit test apparatus for testing a logic circuit having a plurality of input terminals and a plurality of output terminals, the logic circuit test apparatus including: a common test signal generating circuit which groups the input terminals of the logic circuit on the basis of logic states of original test signals to be applied to the respective input terminals of the logic circuit and outputs common test signals from common test signal output terminals thereof smaller in number than the input terminals of the logic circuit; and an input connection switching circuit which switches connections of the common test signal output terminals of the common test signal generating circuit with the input terminals of the logic circuit so as to convert the common test signals into the original test signals and apply the original test signals to the respective input terminals of the logic circuit.